REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated August 11, 2004.

By the present Amendment, the original claims 1-10 have been canceled, without prejudice, and replaced by new claims 11-26. These new claims have been directed to the feature of the invention that are shown, for example, in embodiments such as Figs. 7 and 12 (noting that reference to these particular figures is solely for purposes of example, and not intended to limit the invention only to these examples). Also by the present Amendment, a minor drawing error has been corrected, and a Substitute Specification and a new Abstract have been provided to correct minor informalities noted in review of the application. The undersigned attorney hereby states that no new matter is added by the Substitute Specification.

Briefly, the present claimed invention is directed to providing an improved semiconductor device such as a trench type static induction transistor (SIT) or junction FET (JFET) which overcome prior art problems such as a low drain voltage blocking affect during the off state (as discussed on page 2, lines 3 et seq.). Typically, such transistors are formed of silicon carbide (SiC) which has about ten times as high a dielectric breakdown field as silicon. Referring to Fig. 7 (solely for purposes of example), such a transistor can include a substrate region 11 (serving as a drift region) a drain region 10 (with a corresponding drain electrode 21), source regions 12 formed in the upper surface of the substrate, trenches 32, also formed in the upper surface of the substrate 11, and gate regions 13 formed along the sidewalls and bottoms of the trenches. In particular, as discussed on page 11, line 8

et seq., in the embodiments such as Figs. 7 and 12, in order to extend the channel length of the device, the gate regions can extend from the bottom of the trenches and along the sidewalls of the trenches to contact the source regions 12.

Another feature of the present invention, shown in Figs. 7 and 12, for example, is that the narrowest region of the channels formed between the adjacent trenches are formed in the substrate 11 at a lower level than the trench bottoms. In particular, as shown in Fig. 2, by setting the narrowest portion of the channel at a depth deeper than one half the junction depth of the gate regions 13 and the substrate 11, the on-state resistance is decreased, thereby improving the blocking effect (page 3, line 7 et seq.).

Reconsideration and allowance of independent claims 11 and 18 is respectfully requested. By the present Amendment, new independent claims 11 and 18 both clearly define the above noted features of the extending of the gate regions (claim 18) or control regions (claim 11) along the sidewalls of the trench to contact the source region (claim 18) or the second region (claim 11). Although the cited references to Loose, Yokogawa and Chang are all of general interest regarding trench transistor arrangements, none of them teach or suggest the claimed features of extending the control regions (or gate regions) over the sidewalls of the trench to contact the source region (claim 18) or the second region (claim 11). This is particularly the case when these features are considered in combination with the other claimed features set forth in independent claims 11 and 18. Accordingly, reconsideration and allowance of independent claims 11 and 18 is respectfully requested.

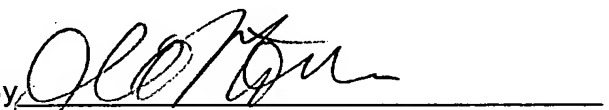
Reconsideration and allowance of dependent claims is also respectfully requested. These claims define additional features of the present invention which serve to even further define over the cited prior art. In particular, claims such as claims 14, 15 and 23-26 particularly define the details of the control/gate regions, which are clearly not taught nor suggested by the cited prior art. Accordingly, reconsideration and allowance of these dependent claims is also respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.43193X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By 

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AMENDMENTS TO THE DRAWINGS

The attached sheet of drawing includes changes to Fig. 14. This sheet, which includes Fig. 14, replaces the original sheet including Fig. 14. In Fig. 14, the lead line for the index line 136 has been corrected, noting that the original lead line was incorrect in showing the control region 136 as being in the p+ gate region 13. The annotated and replacement drawing are attached hereto as Appendix A.

FIG. 13

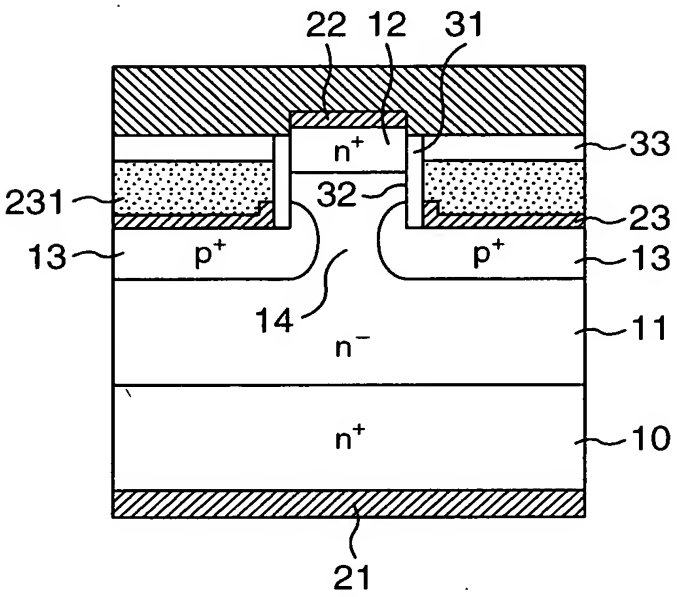
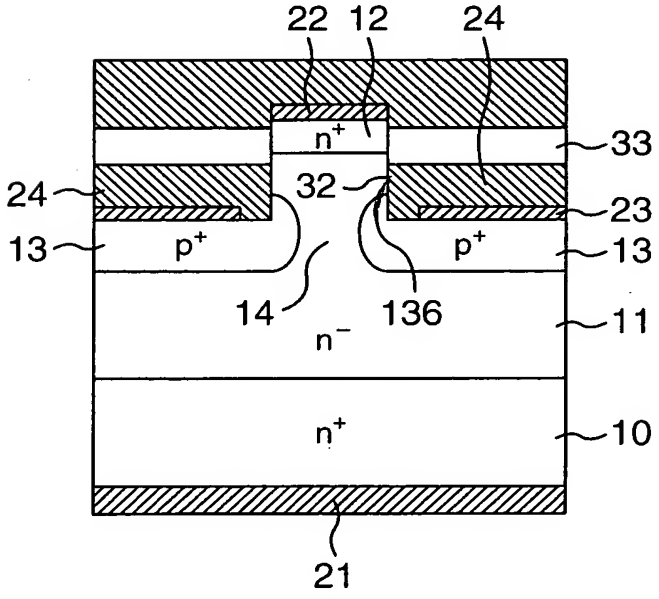


FIG. 14



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SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to improvements for on a structure of transistors such as junction FETs (JFETs) and static induction transistors (SITs).

Silicon carbide (SiC) has about 10 times as high a dielectric breakdown field as silicon (Si), so that a drift region provided to maintain the a blocking voltage can be made thin and highly concentrated, thus reducing a loss of. Power semiconductor devices using SiC include junction FETs (JFETs) and static induction transistors (SITs). An example structure of an SIT that takes advantage of the features of SiC is described in JP-A-2001-94120. The structure in this Japanese patent reference has an n^+ drain region, an n^- drift region, an n^+ source region, a p-type gate region and a p^+ contact region. It also has a drain electrode, a source electrode and a gate electrode. The SIT is are a transistor that turns an electric current on or off by a depletion layer expanding from the gate into a channel. By narrowing the channel width, which is equivalent to an interval between the p-type gate regions, a normally-off capability to maintain an off-state is realized even when a gate voltage is 0 V. The channel is an area between the p-type gate regions, and a thickness of the p-type gate regions represents a channel length. In

the p-type gate region, the depletion layer spreading from the shallow contact region toward the n^--type drift region is not involved in the current control. When an impurity concentration in the p-type gate regions on each side of the channel is low, since the depletion layer expands not only on the channel side but also in the p-type region, a drain voltage blocking effect is weak during the off-state. Therefore, the channel needs to be formed to have an extremely fine width to realize a high blocking voltage.

More specifically, let us consider a case of an SIT with a blocking voltage of several hundred volts. If the thickness of the p-type gate region or the channel length is about 0.5 μm, the channel width needs to be 0.3 μm or less to secure an on-state interruption capability. The p-type gate region requires a junction depth of about 1 μm. To obtain a junction of such a depth, ion implantation must be performed with a large acceleration energy. It is conceivable to use an energy as high as a MeV level in the ion implantation. Such a high energy ion implantation, however, requires a thick mask material for shielding, so that for a fine channel it is necessary to form a fine line with a large aspect ratio with a photolithography process, making the formation of fine channels more susceptible to process variations. If we take process variations to be ±0.05 μm, the on-state voltage and the blocking voltage are both susceptible

to the effect of the process variations, resulting in characteristic variations including a desired blocking voltage failing to be produced or a current failing to flow even during the on-state due to a too narrow channel.

SUMMARY OF THE INVENTION

An object of this invention is to realize a semiconductor device with a reduced on-state resistance and an improved blocking effect, both achieved by an ion implantation with a relatively low energy.

To enhance the gate blocking effect, it is effective to narrow a channel width. Suppressing an ingress of electric field from the drain side is particularly important. It is therefore not necessary to narrow the width over the entire range in the channel depth direction. However, it is important that the channel width be made smaller on the drain side. Further, if the concentration of the p-type gate region is low, the potential barrier expanding from the p-type gate region will decrease even at a low drain voltage, eliminating the blocking effect.

In one aspect the present invention provides a semiconductor device which comprises a trench formed in a second plane of a drift region; a p-type gate region formed from a bottom of the trench into the drift region; a gate electrode formed in the gate region; and a source electrode formed over the gate

electrode through an insulating film.

In another aspect the present invention provides a semiconductor device including: a substrate of a first conduction type with a low impurity concentration and a band gap of 2.0 eV or higher; a first region formed in a first plane of the substrate and having the same conduction type as and a lower resistance than the substrate; a first electrode formed in another plane of the first region; a second region formed in a second plane of the substrate and having the same conduction type as the substrate; and a second electrode formed in the second region; the semiconductor device comprising: a trench formed in the second plane of the substrate; a control region formed from a bottom of the trench into the substrate and having a different conduction type than that of the substrate; a control electrode formed in the control region; and the second electrode formed over the control electrode through an insulating film.

In still another aspect the present invention provides a semiconductor device including: an n-type drift region with a low impurity concentration and a band gap of 2.0 eV or higher; an n-type drain region formed in a first plane of the drift region and having a lower resistance than the drift region; a drain electrode formed in another plane of the drain region; an n-type source region formed in a second plane of the drift region; and a source electrode formed in the

source region; the semiconductor device comprising: a trench formed in the second plane of the drift region; a p-type gate region formed from a bottom of the trench into the drift region; a gate electrode formed in the gate region; and the source electrode formed over the gate electrode through an insulating film.

As described above, as means for not using a high-energy ion implantation, this invention forms a trench in the surface of the substrate on the source side and provides a p-type gate region and a gate electrode in at least the bottom of the trench. This allows the channel width on the drain side to be narrowed even with a low energy ion implantation, thus enhancing the blocking effect of the gate.

Further, by forming an insulating film on the gate electrode to form a source electrode over the entire surface of the unit device, it is possible to minimize an increase in the source electrode resistance even when the device pattern is microfine. This in turn realizes a further reduction in the on-state resistance.

Other objects, features and advantages of the invention will become apparent from the following description of the embodiments of the invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view showing a

structure of an SIT as a first embodiment of the present invention.

Fig. 2 is a graph showing an impurity concentration profile in the first embodiment of the invention.

Fig. 3 is a graph showing a relation between a blocking voltage/on-state resistance and a channel's narrowest portion depth to junction depth ratio.

Fig. 4 is a cross-sectional view showing a structure of an SIT as a second embodiment of the present invention.

Fig. 5 is a cross-sectional view showing a structure of an SIT as a third embodiment of the present invention.

Fig. 6 is a cross-sectional view showing a structure of an SIT as a fourth embodiment of the present invention.

Fig. 7 is a cross-sectional view showing a structure of an SIT as a fifth embodiment of the present invention.

Fig. 8 is a cross-sectional view showing a structure of an SIT as a sixth embodiment of the present invention.

Fig. 9 is a cross-sectional view showing a structure of an SIT as a seventh embodiment of the present invention.

Fig. 10 is a cross-sectional view showing a structure of an SIT as an eighth embodiment of the

present invention.

Fig. 11 is a cross-sectional view showing a structure of an SIT as a ninth embodiment of the present invention.

Fig. 12 is a cross-sectional view showing a structure of an SIT as a tenth embodiment of the present invention.

Fig. 13 is a cross-sectional view showing a structure of an SIT as an eleventh embodiment of the present invention.

Fig. 14 is a cross-sectional view showing a structure of an SIT as a twelfth embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Now, embodiments of the present invention will be described in detail by referring to the accompanying drawings.

Fig. 1 is a cross-sectional view showing a structure of a SIT as a first embodiment of this invention. In the figure, denoted 11 is an n-type drift region, a substrate of first conduction type with a low impurity concentration. An n^+ drain region 10 is a first region formed on a first plane of the n-type drift region (substrate) 11 which has the same conduction type n as, and a lower resistance than, the drift region 11. An n-type source region 12 is a second region formed on a second plane of the substrate

11 which has the same conduction type n as the substrate 11. Reference number 32 designates a trench formed in the second plane of the drift region (substrate) 11. Spreading from a bottom of this trench 32 into the substrate 11 is a gate region 13, a control region of a conduction type p different from that of the substrate 11. Formed over this control region 13 is a gate (control electrode) 23, over which is formed a source 22 (second electrode) through an insulating film 33. Denoted 221 is a source (second unit electrode) and 21 a drain (first electrode).

In this embodiment, the source region 12 was formed over an entire function area of the device through an ion-implantation of nitrogen and then dry-etched to form the trench 32 in 1 μm deep. The bottom of the trench 32 was ion-implanted with aluminum with an acceleration energy of 350 keV at maximum to form the p-type gate region 13. The interval between the trenches 32 (width of the n^+ source region 12) is 0.5 μm. As a result, a junction deeper than 1 μm was able to be formed without using as high an energy as 1 MeV.

Fig. 2 is an impurity concentration profile in the first embodiment used to explain the action of the present invention. A junction depth D is about 1.4 μm and a depth of a narrowest portion of the channel 14 is about 1 μm, approximately 70% of the junction depth D.

Fig. 3 shows a relation between measurements of blocking voltage/on-state resistance and a ratio of the channel's narrowest portion depth to junction depth. The blocking voltage sharply decreases as the depth ratio becomes smaller than 0.5. The dependence of on-state resistance on the depth ratio is not so large as that of the blocking voltage, and an increase of the on-state resistance is not conspicuous even when the depth ratio is larger than 0.5. Therefore, by making the depth of the channel's narrowest portion greater than one-half of the junction depth, the blocking performance can be improved without causing a significant increase in the on-state resistance.

In the first embodiment of this invention, as described above, the narrowest portion of the channel 14 has a depth of about 1 μm, which is about 70%, or sufficiently greater than one-half, of the junction depth. This has resulted in good characteristics. For example, with this first embodiment, ~~That is,~~ a blocking voltage of 600 V or higher was produced with a gate reverse bias of 15 V and the on-state resistance was 1 $m\Omega \cdot cm^2$.

Fig. 4 is a cross-sectional view showing a structure of an SIT as a second embodiment of the present invention. In this embodiment, by applying an inclined ion implantation method in forming the p-type gate region 13, a sidewall of the trench 32 was also formed with a p-type gate region 131. As a result, good characteristics were

produced, such as 600 V or higher blocking voltage obtained with a gate reverse bias of 10 V and 1.2 $m\Omega \cdot cm^2$ on-state resistance.

Fig. 5 is a cross-sectional view showing a structure of an SIT as a third embodiment of the present invention. In this embodiment, the inclined ion implantation on the sidewall of the trench 32 in the second embodiment is performed with a reduced energy lower than 300 keV. This enables the width of the p-type gate region 13 to be formed narrower on a source side 133 than on a drain side 132.

As a result, good characteristics were produced, such as 600 V or higher blocking voltage obtained with a gate reverse bias of 5 V and 1.5 $m\Omega \cdot cm^2$ on-state resistance.

Fig. 6 is a cross-sectional view showing a structure of an SIT as a fourth embodiment of the present invention. In this embodiment, a p-type gate region 134, in the sidewall of the trench 32, ~~in the second embodiment of~~ as shown in Fig. 4, was formed in contact with the n^+ source region 12. This is because the high dielectric breakdown field of SiC makes it possible to secure a sufficient blocking voltage even with a highly concentrated p-n junction.

As a result, it was possible to elongate the channel length that can be controlled by the gate voltage, producing good characteristics. That is, a 600 V or higher blocking voltage was obtained with a

gate reverse bias of 2.5 V and the on-state resistance was 1.7 $m\Omega \cdot cm^2$.

Fig. 7 is a cross-sectional view showing a structure of an SIT as a fifth embodiment of the present invention. In this embodiment, in addition to the third embodiment of Fig. 5, the p-type gate region 135 in the sidewall of the trench 32 was formed in contact with the n^+ source region 12. This allows the length of the channel 14 that can be controlled by the gate voltage to be increased, producing a 600 V or higher blocking voltage without a gate reverse bias. The on-state resistance was 2 $m\Omega \cdot cm^2$.

Fig. 8 is a cross-sectional view showing a structure of an SIT as a sixth embodiment of the present invention. In this embodiment, the sidewall of the trench 32 of the first embodiment of Fig. 1 was oxidized to form a sidewall 331 of insulating film. In this embodiment also, good characteristics similar to those of the first embodiment of Fig. 1 were obtained.

Fig. 9 is a cross-sectional view showing a structure of an SIT as a seventh embodiment of the present invention. In this embodiment, the sidewall of the trench 32 of the second embodiment of Fig. 4 was oxidized to form a sidewall 332 of insulating film. In this embodiment also, good characteristics similar to those of the second embodiment of Fig. 4 were obtained.

Fig. 10 is a cross-sectional view showing a structure of an SIT as an eighth embodiment of the present invention. In this embodiment, the sidewall of the trench 32 of the third embodiment of Fig. 5 was oxidized to form a sidewall 333 of insulating film. In this embodiment also, good characteristics similar to those of the third embodiment of Fig. 5 were obtained.

Fig. 11 is a cross-sectional view showing a structure of an SIT as a ninth embodiment of the present invention. In this embodiment, the sidewall of the trench 32 of the fourth embodiment of Fig. 6 was oxidized to form a sidewall 334 of insulating film. In this embodiment also, good characteristics similar to those of the sixth embodiment were obtained.

Fig. 12 is a cross-sectional view showing a structure of an SIT as a tenth embodiment of the present invention. In this embodiment, the sidewall of the trench 32 of the fifth embodiment of Fig. 7 was oxidized to form a sidewall 335 of insulating film. In this embodiment also, good characteristics similar to those of the seventh embodiment were obtained.

Fig. 13 is a cross-sectional view showing a structure of an SIT as an eleventh embodiment of the present invention. In this embodiment, in addition to the first embodiment of Fig. 1, the sidewall of the channel 14 in contact with the sidewall of the trench 32 was formed as a MOS channel. In the figure, numeral 1 denoted

31 denotes a gate insulating film, and numeral 231 denotes a MOSFET gate formed of a low-resistance polysilicon or metal such as aluminum. In this embodiment, of the channel region 14 between the control regions 13, the sidewall portion adjoining the sidewall of the trench 32 is formed as a MOS channel. The provision of the MOSFET in the channel 14 improves the off-state characteristic as well as the normal SIT operations. At the same time, a positive voltage is applied to the gate during the on-state to form a conductive MOS channel in the sidewall of the trench 32 to improve the on-state characteristic.

As a result, good characteristics were produced. That is, a 600 V or higher blocking voltage was obtained without a gate reverse bias. The on-state resistance was 1.7 $m\Omega \cdot cm^2$.

Fig. 14 is a cross-sectional view showing a structure of an SIT as a twelfth embodiment of the present invention. In this embodiment, in addition to the first embodiment of Fig. 1, the sidewall of the channel 14 was formed with a MESFET. In the figure, numeral 24 denotes a Schottky gate of the MESFET. Thus, the control region 136 adjoining the sidewall portion of the trench 32 forms a Schottky contact at the sidewall portion. In this embodiment, the provision of the MESFET in the channel 14 can improve the off-state characteristic as well as the normal SIT operations. At the same time, a positive voltage is applied to the

gate during the on-state to form a conductive MOS channel in the sidewall of the trench 32 to improve the on-state characteristic.

With this construction, good characteristics were produced. That is, a 600 V or higher blocking voltage was obtained without a gate reversed bias, and the on-state resistance was 1.5 $m\Omega \cdot cm^2$.

Since the above embodiments can realize a low gate reversed bias and a low on-state resistance, there are advantages, when they are applied to inverter switching devices, that the gate driving becomes easy and loss can be reduced. Also, even though the ion implantation is carried out with a relatively low energy, this invention can realize a semiconductor device with a reduced on-state resistance and an improved blocking effect.

It should be further understood by those skilled in the art that although the foregoing description has been made on various embodiments of the invention, the invention is not limited thereto, and various changes and modifications may be made without departing from the spirit of the invention and the scope of the appended claims.